

FIG. 1



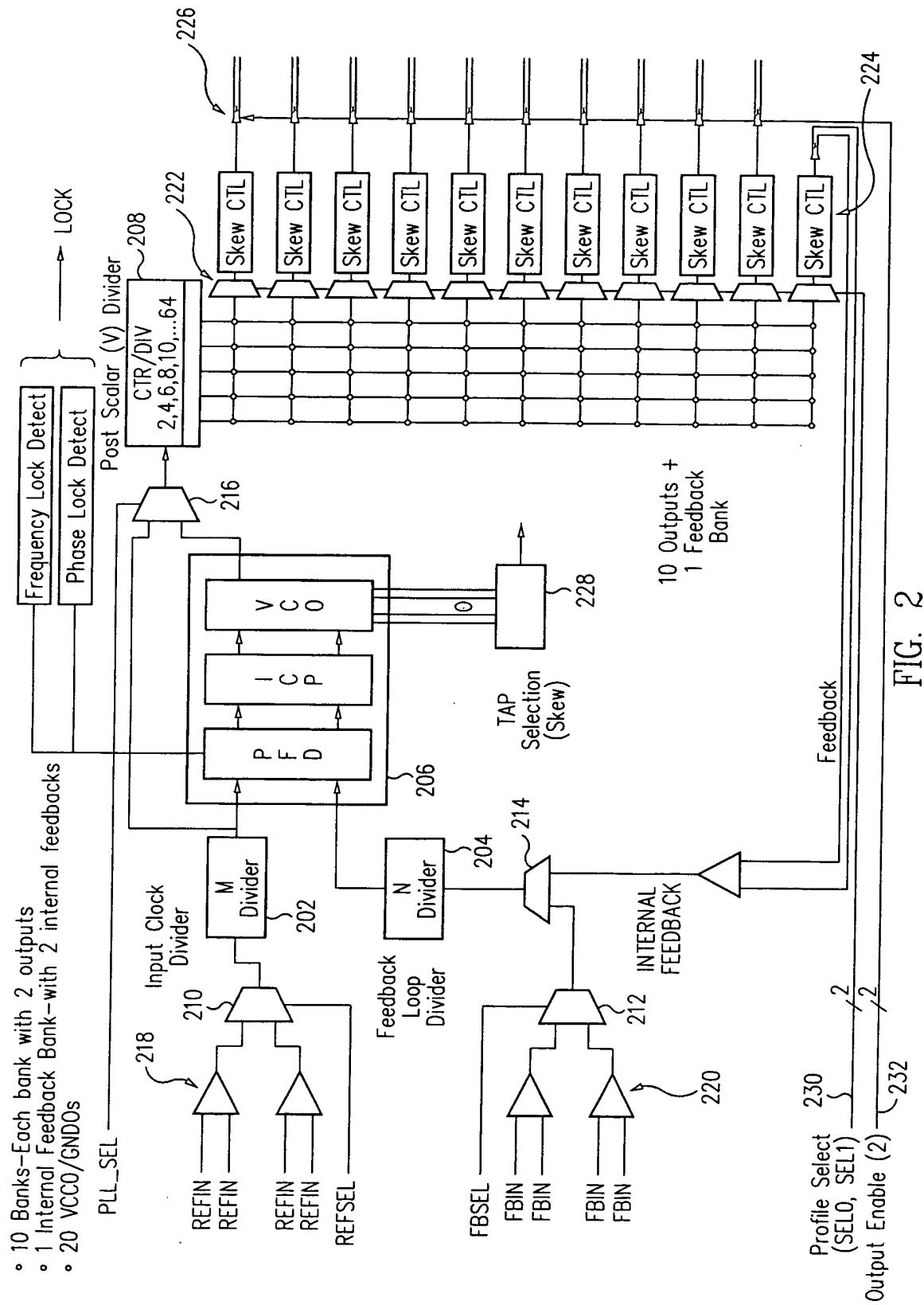


FIG. 2

External Frequency Select Control & Five Different Frequency Generations

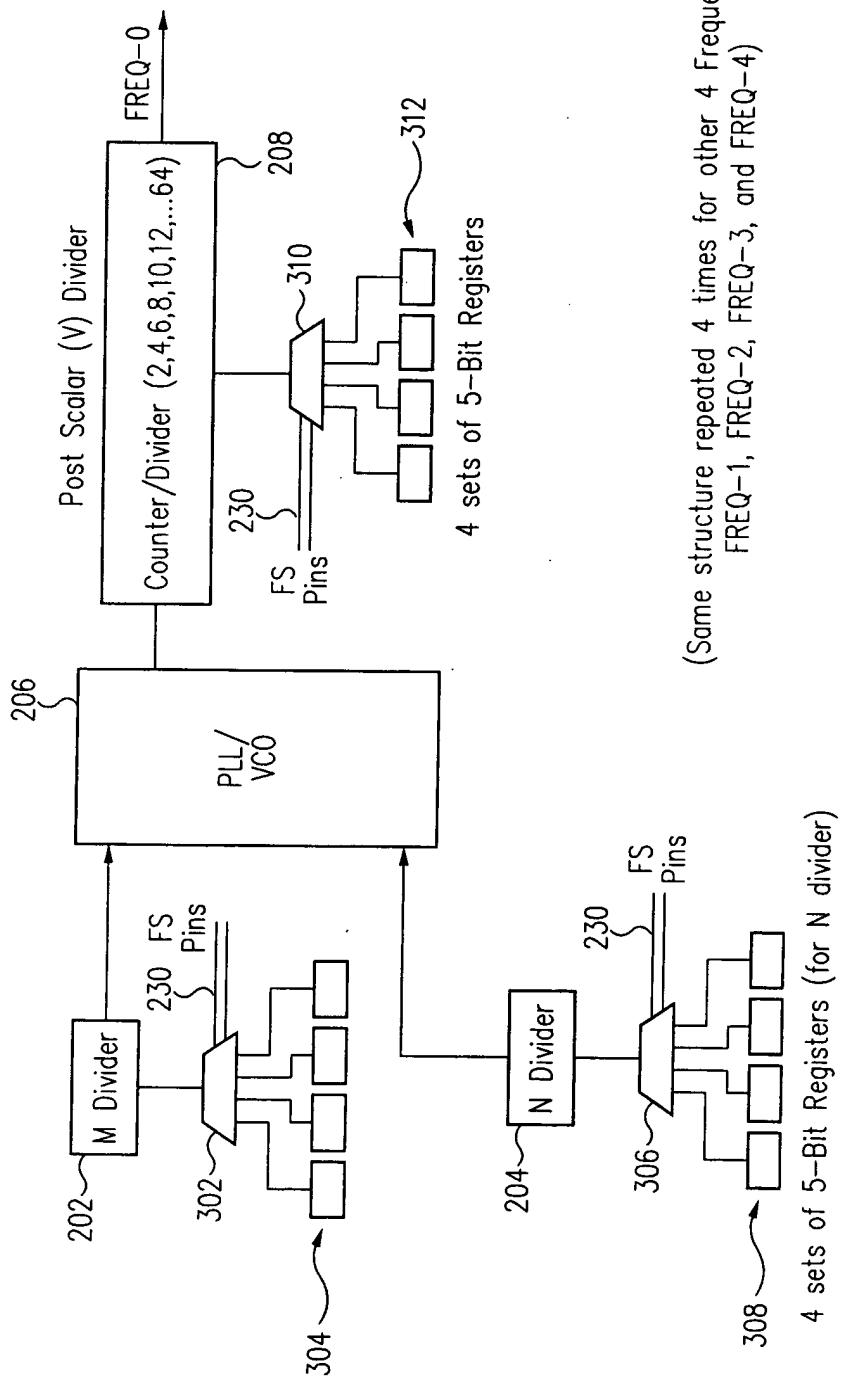


FIG. 3

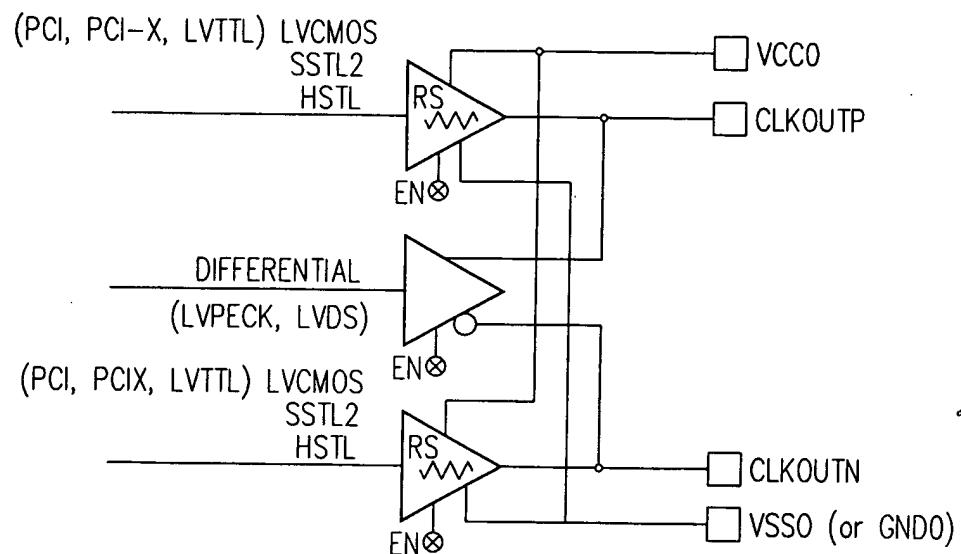


FIG. 5

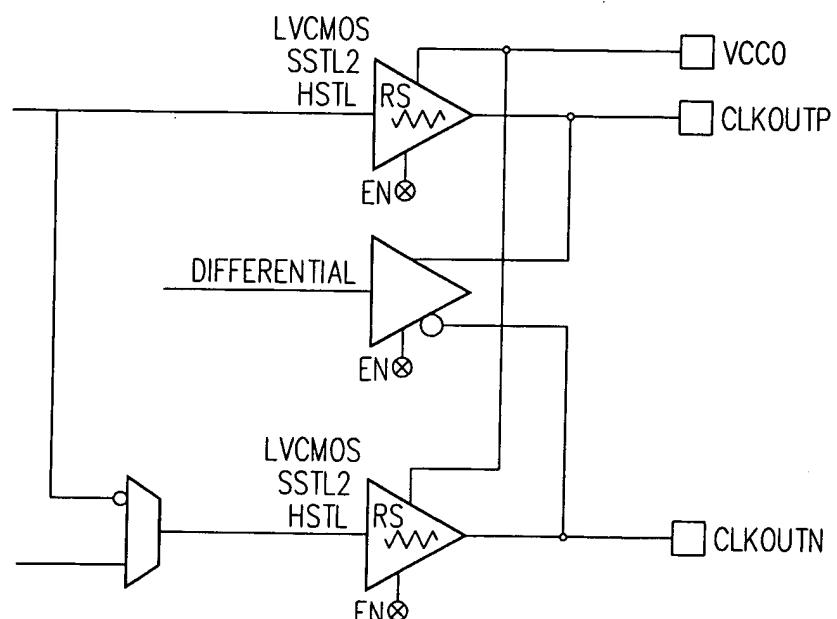


FIG. 6

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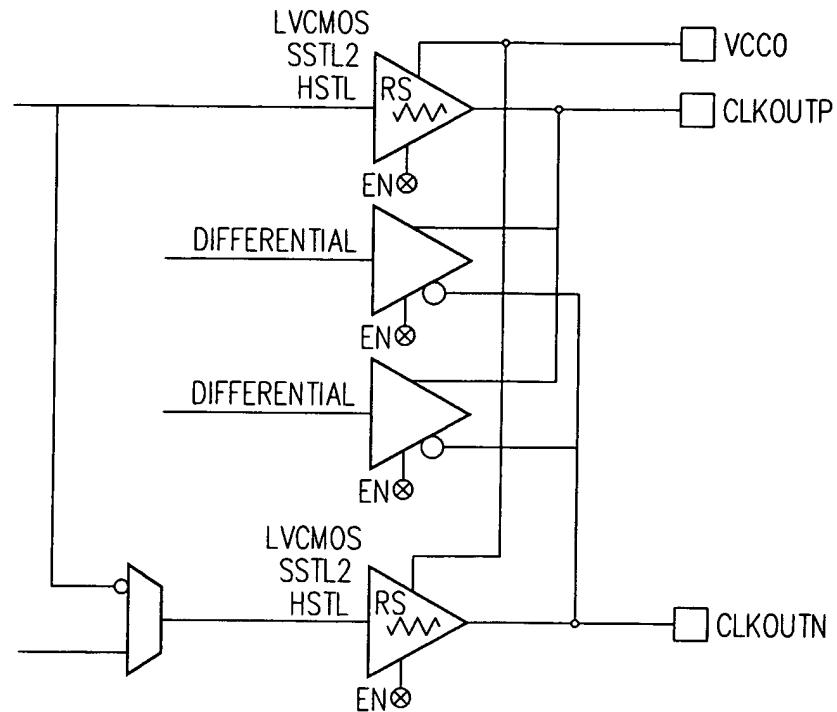


FIG. 7

Reference clock input stage

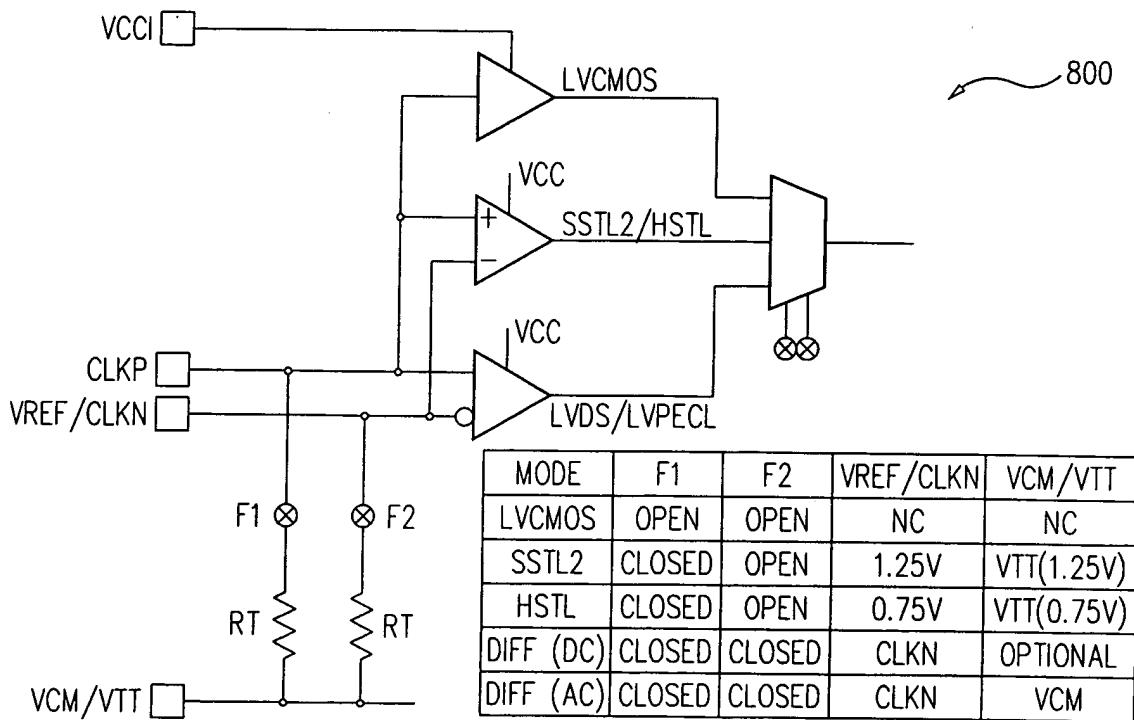


FIG. 8

SSTL2/HSTL input application

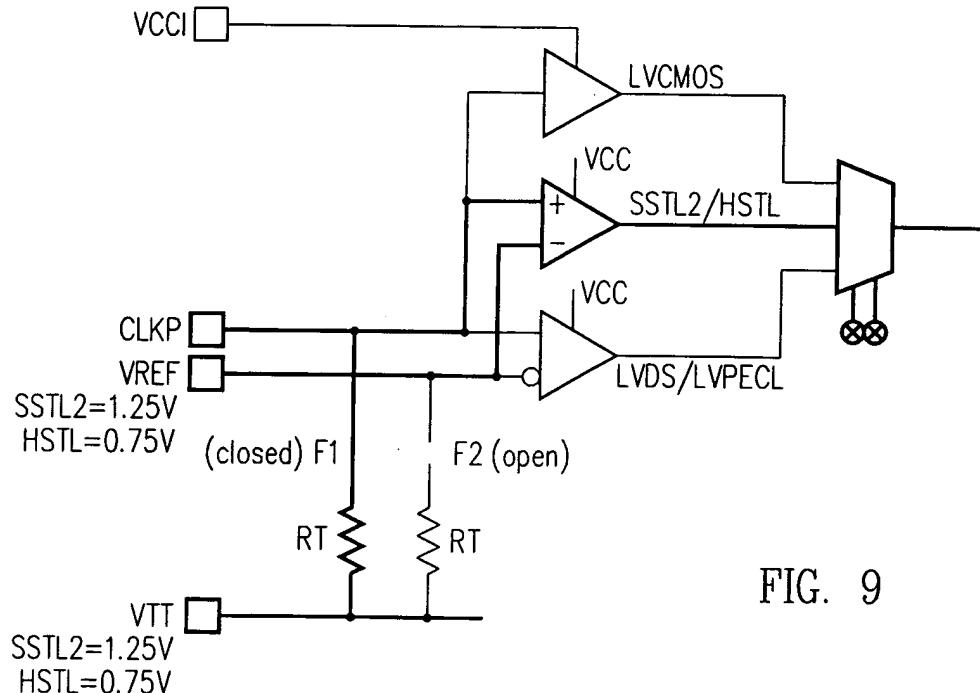


FIG. 9

Alternative DC coupled differential application

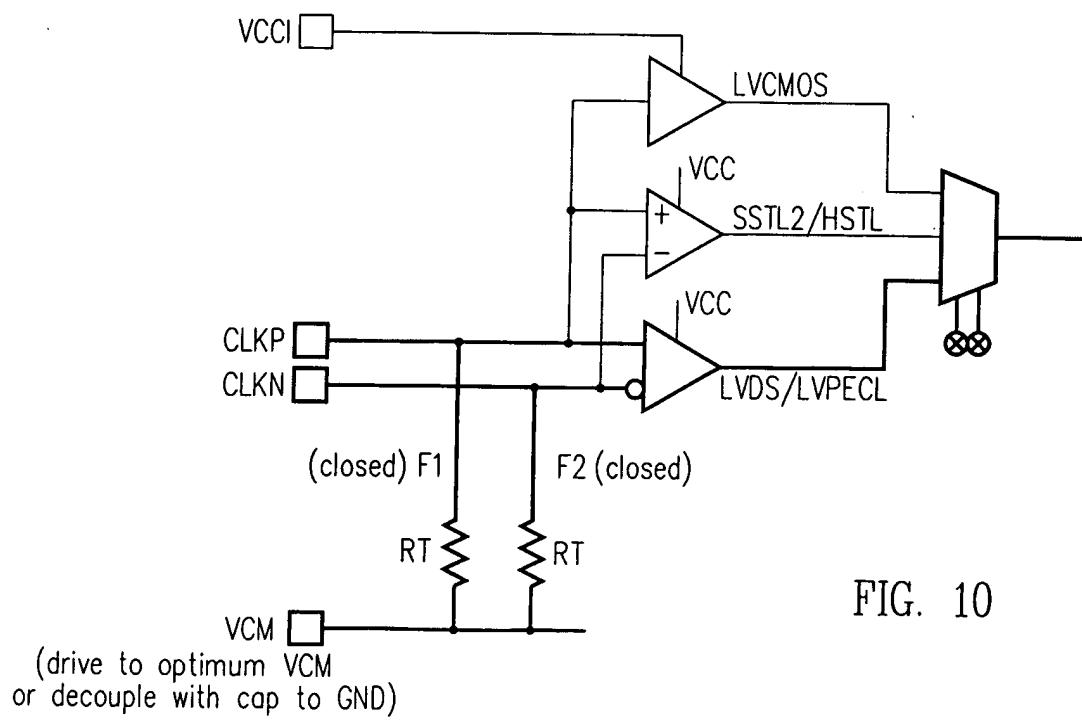


FIG. 10

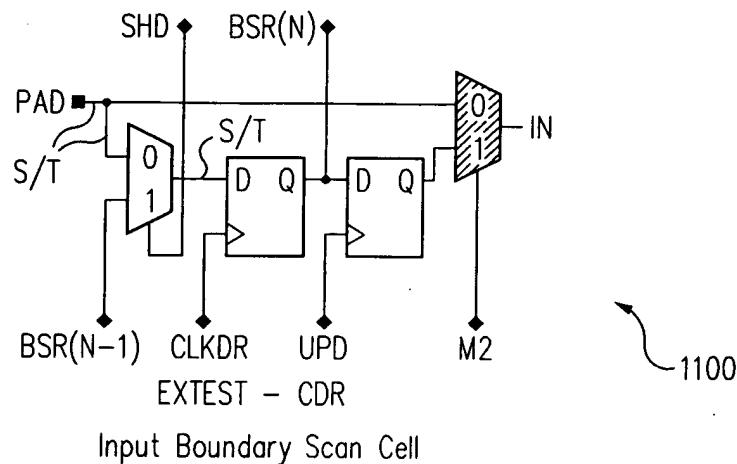


FIG. 11

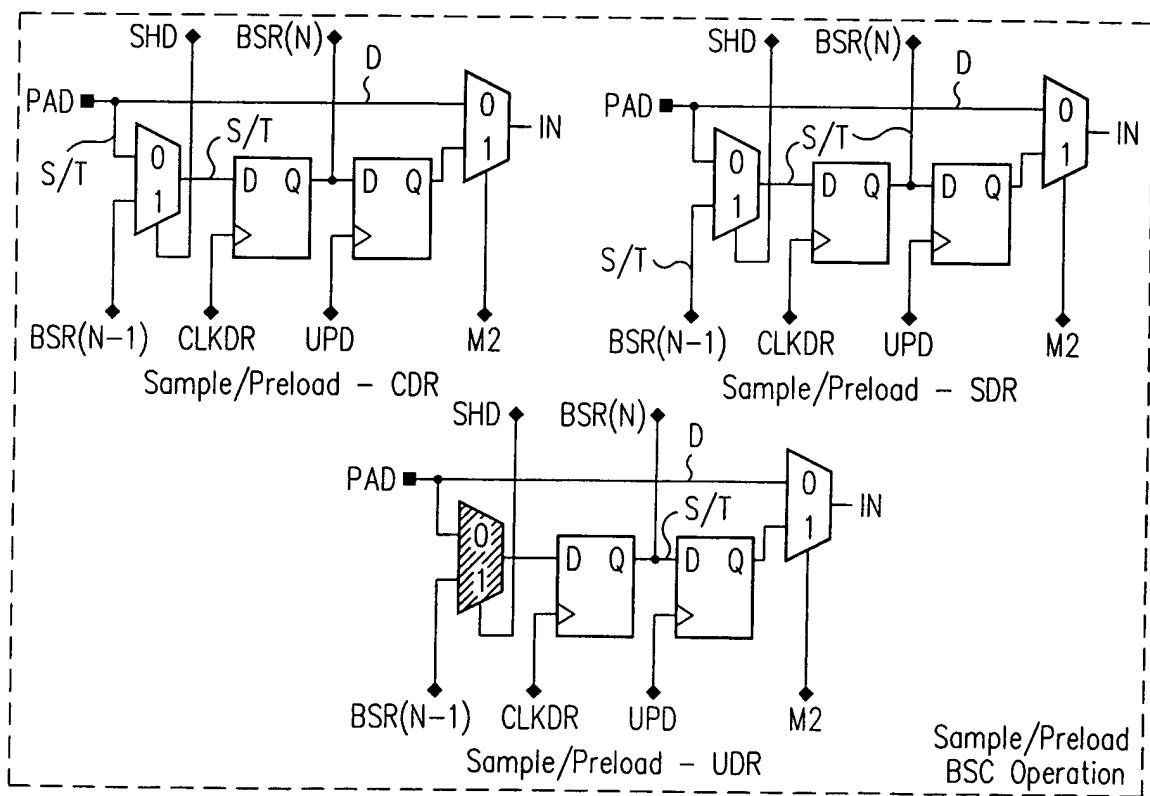


FIG. 12

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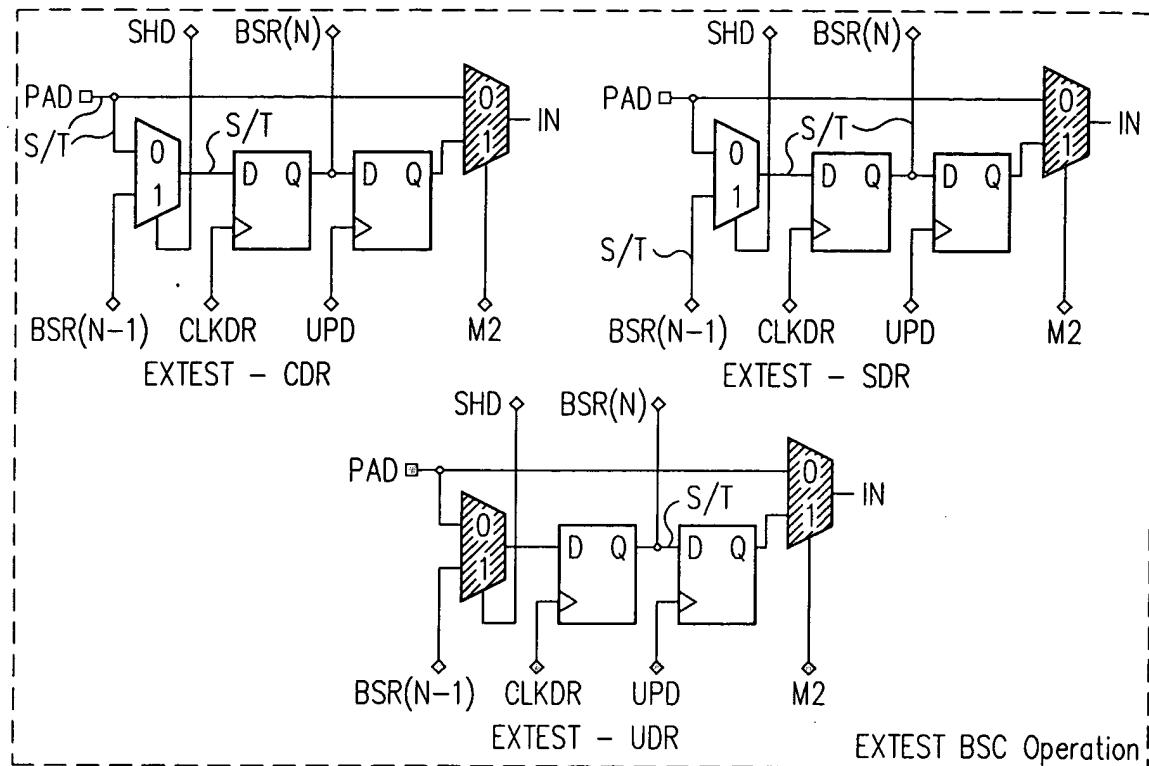


FIG. 13

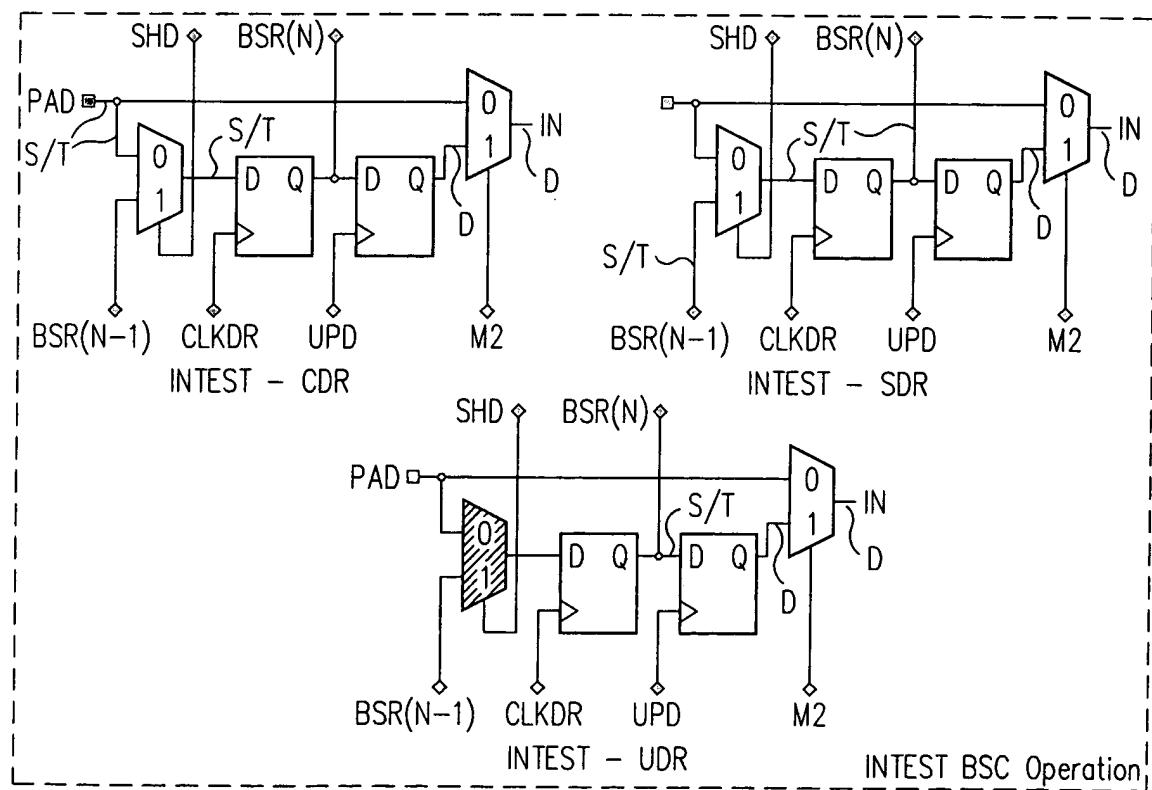


FIG. 14

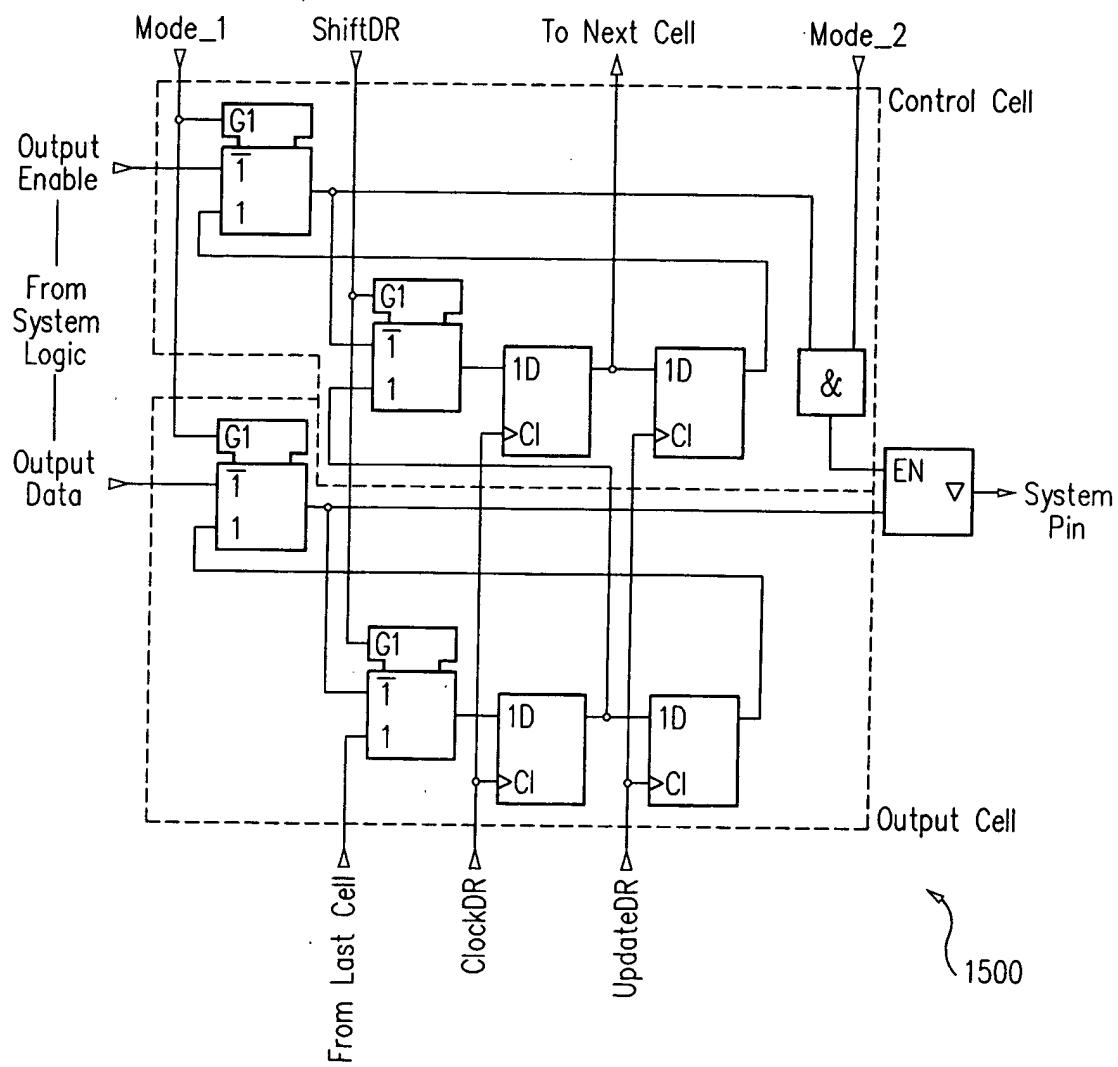


FIG. 15